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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/600,259	06/20/2003	Jeffrey Lutze	SNDK.310US0	7482

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EXAMINER	
LE, THAO P	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 02/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/600,259	LUTZE ET AL.	
	Examiner	Art Unit	
	Thao P. Le	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/29/04*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12 and 18-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *20-23* is/are allowed.

6)☒ Claim(s) *1-12,18 and 19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/13/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

Information Disclosure Statement (IDS) filed on **12/29/04** and made of record. The references cited on the PTOL 1449 form have been considered.

Claims 1-12, 18-23 are pending in this application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1, 6-7, 18-19 are rejected under 35 USC 102 (a) as being anticipated by Chiu et al., U.S. Patent No. 6562682.

Regarding claim 1, Chiu et al. discloses a method of making an array of non-volatile memory cells on a substrate comprising: forming an array of first floating gate portions 202, gate dielectric (tunnel oxide), opening 208 using a mask layer 206 not covered by first floating gate portions 202 and is self-aligned to the first floating gate portions, forming sidewall 210, forming second floating gate portions 214 defined by the

sidewall elements in at least one direction and contacting the first floating gate portion 202 (See. Figs.1-2).

Regarding claim 6, Chiu et al. discloses the sidewall portions are formed by deposition and etch back of silicon nitride (210, 2B-2C).

Regarding claim 7, Chiu et al. discloses the second floating gate portions are formed by deposition and etch back of polysilicon.

Regarding claim 18, Chiu et al. discloses a method of making an array of non-volatile memory cells on a substrate comprising: forming an array of first floating gate portions 202 wherein each first floating gate portion is inherently separated from adjacent first floating gate portions; forming second floating gate portions 214 wherein each second floating gate portion extends along a plane perpendicular to the plane of the substrate surface and wherein the plane of the second floating gate portion bisects the first floating gate portion (Figs. 1-2).

Regarding claim 19, Chiu et al. discloses the first portion is square and the second portion is about midline of the first portion (Fig. 2E).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the

subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-5, 8-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiu et al., U.S. Patent No. 6562682, in view of Chuang et al., U.S. Pub No. 2004/0033663.

Regarding to claim 2, Chuang et al. discloses the forming of gate dielectric 202 on a substrate and forming a layer of gate material 203 on the gate dielectric (Fig. 2c). It would have been obvious to one having ordinary skill in the art at the time the invention was made to form a layer of dielectric material over the layer of gate material and etching both layer in the same pattern to form first floating gate portions covered by dielectric material in order to protect the underlying floating gate material from etching and reducing the method step.

Regarding to claim 3, it is inherent that for devices in Chiu and Chuang et al., source/drain regions are required and source/drain regions are formed by implanting impurities and formed into the substrate besides the gate.

Regarding claims 4-5, Chuang et al. discloses the masking layer is formed and portion that lies over the gate portion is removed (Fig. 2a) and the dielectric material is removed after the mask layer is removed (Fig. 2e).

Regarding claim 8, Chuang et al. discloses the steps of removing the sidewall elements thereby exposing surfaces of the first and second floating gate portions (Fig. 2H), forming a dielectric layer on the exposed floating gate portion surfaces, forming a dielectric layer 211 (Fig. 2i) on the exposed floating gate portion surfaces and forming conductive gtes 212 (Fig. 2i, para 0037) extending across the floating gates in at least one direction and in contact with the dielectric layer. It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Chiu et al. in view of Chuang et al. because the structure of Chiu et al. requires dielectric material formed over the floating gate portion for insulation between floating gate material and conductive material that is formed on the dielectric material to electrically connecting the floating gate material with other devices.

Regarding claim 9, it is well known in the art at the time the invention was made that ONO layer is used as dielectric material in floating gate structure.

Regarding claims 10-11, Chuang et al. discloses the conductive gates extend towards the surface of the semiconductor substrate such that the lowest extremities of the conductive gates are closer to the surface of the semiconductor substrate than the highest extremities of the second floating gate portions (claim 10) and wherein the conductive gates extend the enclose the second floating gate portions from above and on four lateral sides (claim 11) (See Fig. 2i).

Regarding claim 12, Chiu and Chuang et al. fail to disclose the step of forming a metal on the conductive/control gate 212 in order to form silicide layer. However, it is

well known in the art that silicide layer is formed on the control gate in non-volatile memories to reduce resistivity of the gate.

References cited in PTO-892 also disclose similar method of forming non-volatile memory cells as recited in claims 1-12, 18-19.

When responding to the office action, Applicants' are advice to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Allowable Subject Matter

Claims 20-23 are allowed.

None of the references of record teaches or suggests the claimed limitations having a method of forming a non-volatile memory cells on a semiconductor substrate surface comprising, among other steps cited in independent claim 20, the steps of forming a layer of floating gate material extending across the layer of gate dielectric, forming shallow trench isolation structures that divide the layer of floating gate material into strips and extend in

one direction, forming a plurality of first masking strips and the first masking strips extending in a second direction that is perpendicular to the first direction, forming a plurality of second masking strips that fill spaces between first masking strips, forming spacers along sidewalls of the second masking strips which extending in the second direction, and then forming second floating gate portions by filling gaps between spacers of adjacent second masking strips.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao P. Le whose telephone number is 571-272-1785. The examiner can normally be reached on M-T (7-6).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thao P. Le
Examiner
Art Unit 2818